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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/916,509	07/30/2001	Katsuhiko Hieda	04329.2613	8843

7590 10/24/2002

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EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 10/24/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/916,509	HIEDA, KATSUHIKO	
	Examiner	Art Unit	
	Thao X Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) *3-21 and 24-34* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,23 and 35-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claim 22 is cancelled in Paper No 8.

Drawings

2. Figures 79-81 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 23, 35-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 5,567,962 to Miyawaki et al.

Regarding to claim 1, Miyawaki discloses a semiconductor device comprising a convex semiconductor layer 1013/1016/1021, fig 17, provided on a semiconductor substrate, a source region 1030, column 10 line 32, and a drain region 1017 column 9 line 59 in the convex semiconductor layer, and a gate electrode 1023, column 10 line 11 having side-wall gate portion 1023, 1086 fig. 12, and column 6 line 53-61, provided over a side a side surface of the convex semiconductor layer, the side-wall gate portion being offset

with respect to a part of a lower portion of the source region and a part of a lower portion of the drain region, fig. 14.

But, Miyawaki does not expressly disclose in an insulated state with respect to the convex semiconductor layer, the gate electrode applying an electric field effect to a channel region between the S/D regions, via at least the side surface of the convex semiconductor layer. However, it would have been obvious to one of ordinary skill in the art to applying the voltage to the gate electrode to create the electric field effect to a channel region, because such transistor function is well known the art, see David A. Hodges and Horace G. Jackson, Analysis and Design of Digital Integrated Circuits, second Edition, McGraw-Hill, Inc. 1988, page 36. Furthermore, when the structure recited in the reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent. Where the claimed and the prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977).

Regarding to claim 2, Miyawaki discloses a semiconductor device comprising a convex semiconductor layer 1013/1016/1021, fig 17, provided on a semiconductor substrate, a source region 1030, column 10 line 32, and a drain region 1017 column 9 line 59 in the convex semiconductor layer, and a gate electrode 1023, column 10 line 11 having side-wall gate portion 1023, fig. 12, and column 6 line 53-61, provided over a side a side surface of the convex semiconductor layer, and the side-wall insulating film 1022,

fig. 12 column 10 line 9, on a side surface of the gate electrode and the side surface of the convex semiconductor layer.

But, Miyawaki does not expressly disclose in an insulated state with respect to the convex semiconductor layer, the gate electrode applying an electric field effect to a channel region between the S/D regions, via at least the side surface of the convex semiconductor layer. However, it would have been obvious to one of ordinary skill in the art to applying the voltage to the gate electrode to create the electric field effect to a channel region, because such transistor function is well known the art, see David A. Hodges and Horace G. Jackson, Analysis and Design of Digital Integrated Circuits, second Edition, McGraw-Hill, Inc. 1988, page 36. Furthermore, when the structure recited in the reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent. Where the claimed and the prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977). Regarding to claims 23 and 35-45, please refer to previous Office Action Paper No 7.

Response to Arguments

5. Applicant's arguments filed 8/19/02 have been fully considered but they are not persuasive.

a. The Applicant argues that prior art does not discloses gate electrode having side-wall gate portion .... the side-wall gate portion being offset with respect to a part of a lower portion of the source region and a part of a lower portion of the drain region. The Examiner respectfully disagree because the prior art of record shows in fig. 12 and 14, discloses gate electrode 1023 having side-wall gate portion, fig. 12, ... the side-wall gate portion being offset with respect to a part of a lower portion of the source region and a part of a lower portion of the drain region, fig. 14.

b. The Applicant argues that 'it would have been obvious ..... to apply the voltage to the gate electrode to create the electric field effect to the channel region, because such transistor function is well know in the art' would require supporting evidence. The function of transistor can be found the textbook such as David A. Hodges and Horace G. Jackson, Analysis and Design of Digital Integrated Circuits, second Edition, McGraw-Hill, Inc. 1988 for the record.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X Le whose telephone number is 703-306-0208. The examiner can normally be reached on M-f from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Thao X. Le
October 4, 2002

PHAT X. CAO
PRIMARY EXAMINER